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EXAMINER	
CHANG, ERIC	
ART UNIT	**PAPER NUMBER**
2116	14

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/504,003	KAHN ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 and 12-32 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-10 and 12-32 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-21, 24 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,128,747 to Thoulon, in view of U.S. Patent 5,692,204 to Rawson, et al.

5. As to claim 1, Thoulon discloses an apparatus comprising:

[a] a processor [col. 3, line 33];

[b] an operating system to control a plurality of power management states, comprising a low latency low power state [col. 1, lines 33-35];

[c] a memory subsystem that exits a memory low power state [col. 2, lines 37-41]; and

[d] control logic to detect exiting of said low latency low power state and to remove said memory subsystem from said memory low power state prior to allowing execution of processor to resume [col. 5, line 37-47].

Thoulon teaches all of the limitations of the claim, by allowing for resumption of memory operations from a low latency sleep state by means of control logic that does not require BIOS intervention, but does not teach the specific initialization commands required by the memory subsystem to exit the low power state. However, Thoulon teaches that the apparatus wakes the memory from a low power mode [col. 2, lines 60-61], and it would be obvious to one of ordinary skill in the art that if a plurality of initialization commands were required to wake the memory from a low power mode that they would necessarily issued by said taught apparatus. Furthermore, Thoulon teaches that his invention negates the need for the processor itself to specifically issue the commands needed to control the sleep mode of the memory, allowing said commands to be transparently handled by the control logic [col. 3, lines 57-64], substantially as claimed.

Thoulon teaches all of the limitations of the claim but does not teach that a low power state exit message is received from a first component, and that an end of low power state exit message is subsequently sent to the first component.

Rawson teaches that power management event notification messages are passed between components in order to place systems into and out of low power states [col. 1, lines 44-63]. Furthermore, Rawson teaches that these messages may also comprise power state transition completion messages [col. 8, lines 32-34], such as an end of low power state exit message, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ power management event notification messages as taught by Rawson. One of ordinary skill in the art would have been motivated to do so to allow the

memory subsystem to communicate with other components its power state, using a standardized message protocol, instead of solely relying on the detection of sleep assertion signals.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of placing a computer into and out of a low power state. Moreover, the power management event notification means taught by Rawson would improve the flexibility of Thoulon because it allowed the power management functions to centralized by a power management executive for an adaptive approach to power management.

6. As to claim 2, Thoulon discloses the resumption from low power mode is performed by control logic in the memory controller and does not require executing BIOS or other firmware routines [col. 4, lines 2-14].

7. As to claims 3, 14 and 28, Thoulon discloses the low power state is one as defined by the ACPI standard where STPCLK is asserted, as in the S1 state [col. 1, lines 33-47]. Furthermore, Thoulon teaches that during the sleep state, other processes may occur independently of the processor, meaning that although the system is in a low power state, context is maintained, as in the S1 state, substantially as claimed [col. 5, lines 1-6]. Likewise, as described in Applicant's specification [page 4, lines 2-5], resuming from the S1 state occurs without executing BIOS routines.

8. As to claims 4-5, 18 and 24, Thoulon discloses the control logic detects exit from the low power state [col. 4, lines 39-50 and 59-67], and deasserts the stop clock signal after the memory capabilities have been resumed [col. 4, lines 51-58]. Thoulon also teaches that this process occurs transparently to the execution resources of the processor [col. 4, lines 9-14]. Furthermore, Rawson teaches that power management event notification messages are passed between components in order to place systems into and out of low power states [col. 1, lines 44-63], and that these messages may also comprise power state transition completion messages [col. 8, lines 32-34], such as an end of low power state exit message, substantially as claimed.

9. As to claims 6, 10 and 12-13, Thoulon teaches that the sleep control means are incorporated in the memory controller, which may comprise a memory interface and ICH, substantially as claimed [col. 6, lines1-3]. Thoulon also teaches that the sleep control means receives a first low power exit message [col. 4, lines 59-62], and transmits a second end of low power state exit message indicating that the memory initialization is complete [col. 5, lines 17-20]. Thoulon teaches that bus transactions may be used as the means to convey these messages, substantially as claimed. In addition, Thoulon discloses deasserting the stop clock signal after the memory capabilities have been resumed from a low latency sleep state, substantially as claimed [col. 4, lines 51-58]. Furthermore, Rawson teaches that power management event notification messages are passed between components in order to place systems into and out of low power states [col. 1, lines 44-63], and that these messages may also comprise power state transition completion messages [col. 8, lines 32-34], such as an end of low power state exit message, substantially as claimed.

10. As to claims 7-9, 15-17, 19-21, and 29, Thoulon discloses the initialization commands comprise those necessary to control the low power state of the memory are generated by the control logic instead of by the processor or like firmware [col. 3, lines 57-64]. It would be obvious to one of ordinary skill in the art that such commands comprise initializing memory interface control logic and starting and locking a clock, as well as performing whatever necessary current calibration sequences and memory core initialization operations, substantially as claimed. As is well known in the Rambus RDRAM technology, as described in the Rambus Direct RAC Data Sheet submitted by Applicant, performing a current calibration sequence comprises setting control registers [page 73], and the core initialization comprises having the memory banks pre-charged and refreshed for subsequent transactions operations [page 50, column 1], in addition to stabilizing the memory clocks [page 72-73].

11. As to claims 26-27, Thoulon discloses a system comprising:

[a] a processor [FIG 1, element 10];

[b] a memory [FIG 1, element 13];

[c] an I/O controller for generating a first message to exit a low power state and a second message to the processor [col. 4, lines 59-62]; and

[d] a memory controller receiving the first message, initializing the memory and generating a second message to be passed to the processor [FIG 1, element 12, and col. col. 4, lines 59-62, and col. 5, lines 17-20].

Furthermore, Thoulon teaches that the processor and memory controller are part of an integrated processor device [FIG 1].

12. Claims 22-23, 25 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over over U.S. Patent 6,128,747 to Thoulon, in view of U.S. Patent 5,692,204 to Rawson, et al., in further view of over U.S. Patent 6,055,643 to Chaiken.

13. As to claims 22, 25 and 31, Chaiken discloses:

Thoulon and Rawson teach all of the limitations of the claim, but do not teach that a bit is set upon entry into a low latency low power state.

Chaiken teaches reading a bit set upon entry into a low latency low power state and sending a resume message to the memory controller [col. 14, lines 40-56]. Chaiken teaches that a bit in the enable register is set to indicate when the system enters a different power state, and that operating system interrupts, such as a resume message, are generated in response.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the low-power bit as taught by Chaiken. One of ordinary skill in the art would have been motivated to do so that the cause of the resume message is specified.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of placing a computer system into a low power mode. Moreover, the low-power bit means taught by Chaiken would improve the flexibility of Thoulon and Rawson because it allows one or more wake devices to generate the end-of-low-power state.

14. As to claim 23, Thoulon discloses signaling that the memory interface has completed its initialization commands [col. 5, lines 17-20]. In addition, Thoulon discloses deasserting a stop clock signal [col. 4, lines 51-58]. Rawson also teaches that power management event notification messages are passed between components in order to place systems into and out of low power states [col. 1, lines 44-63], and that these messages may also comprise power state transition completion messages [col. 8, lines 32-34], such as an initialization complete message, substantially as claimed.

15. As to claim 32, Thoulon discloses the low power state is one as defined by the ACPI standard where STPCLK is asserted, as in the S1 state [col. 1, lines 33-47]. Furthermore, Thoulon teaches that during the sleep state, other processes may occur independently of the processor, meaning that although the system is in a low power state, context is maintained, as in the S1 state, substantially as claimed [col. 5, lines 1-6]. Likewise, as described in Applicant's specification [page 4, lines 2-5], resuming from the S1 state occurs without executing BIOS routines.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ec

May 7, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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